WHAT IS CLAIMED IS:

1. A processor clock generation circuit for a low power consumption modem chip design, comprising:

a first clock generator for generating a first clock signal in response to enable and disable signals;

a second clock generator for generating a second clock signal that is lower in frequency than the first clock signal;

a decoder for decoding an externally inputted instruction to check whether the inputted instruction is a power-down instruction or a power-up instruction, and generating control signals;

a clock selection unit for, if the instruction is the power-down instruction, outputting the second clock signal as a processor clock signal and outputting a clock change end signal in response to a control signal outputted from the decoder and, if the instruction is the power-up instruction, outputting the first clock signal as the processor clock signal in response to the outputted control signal from the decoder and a first clock wake-up end signal; and

a first clock controller for, if the instruction is the power-down instruction, outputting the disable signal for disabling clock generation of the first clock generator in response to the control signal outputted from the decoder and the clock change end signal outputted from the clock selection unit and, if the instruction is the power-down instruction, outputting the enable signal for enabling the clock generation of the first clock generator in response to the control signal outputted from the decoder, and outputting the first wake-up end signal after a predetermined time.

2. The processor clock generation circuit of Claim 1, wherein the first clock generator includes:

an oscillator for generating the first clock signal; and

a switch for enabling/disabling an operation of the oscillator in response to the enable and disable signals.

3. The processor clock generation circuit of Claim 2, wherein if the instruction is the power-up instruction, the first clock controller outputs the enable signal for enabling clock the clock generation of the first clock generator, and outputs the first clock wake-up end signal after the lapse of an oscillator wake-up time taken until the oscillator outputs the stable first clock signal.

4. The processor clock generation circuit of Claim 1, wherein the clock selection unit includes:

a clock selection signal generator for selecting the second clock signal if the instruction is the power-down instruction and selecting the first clock signal if the instruction is the power-up signal, in response to the control signal outputted from the decoder; and

a multiplexer for outputting one of the first and second clock signals as the processor clock signal in response to the selection signal.

5. The processor clock generation circuit of Claim 1, wherein the decoder, the clock selection unit, and the first clock generator are constructed in one-chip of the processor.

6. The processor clock generation circuit of Claim 1, wherein the modem chip is a code division multiple access (CDMA) modem chip.

7. A method of generating a clock signal for a processor built in a modem chip having a first clock generator for generating a first clock signal and a second clock generator for generating a second clock signal that is lower, in frequency, than the first clock signal, the method comprising:

decoding an externally inputted instruction to check whether the instruction is a power-down instruction and a power-up instruction;

if the instruction is the power-down instruction, then performing a power down method comprising:

selecting a clock signal supplied to the processor as the second clock signal;

generating a clock change end signal; and

controlling the first clock generator to interrupt generation of the first clock signal,

if the instruction is the power-up instruction, then performing a power-up method comprising:

controlling the first clock generator to interrupt generation of the fist clock signal;

counting a wake-up time of the first clock generator;

checking whether the a wake-up count value reaches a preset wake-up end time value;

if the wake-up count value does not reach the preset wake-up end time value, then repeating the counting step; and

if the wake-up count value reaches the preset wake-up end time value, selecting the supplied clock signal as the first clock signal.

8. The method of Claim 7, wherein the wake-up end time is a time required for allowing the first clock generator to output a stable first clock signal.